DATA SHEET

TDA9800
VIF-PLL demodulator and FM-PLL detector

Preliminary specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

FEATURES

- Suitable for negative vision modulation
- Applicable for IF frequencies of 38.9 MHz, 45.75 MHz and 58.75 MHz
- Gain controlled wide band VIF amplifier (AC coupled)
- True synchronous demodulation with active carrier regeneration (ultra-linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response)
- Peak sync AGC for negative modulation
- Video amplifier to match sound trap and sound filter
- AGC output voltage for tuner; adjustable take-over point (TOP)
- AFC detector without extra reference circuit
- Alignment-free FM-PLL detector with high linearity
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- 5 to 8 V positive supply voltage range, low power consumption (300 mW at +5 V supply voltage).

GENERAL DESCRIPTION

The TDA9800 is a monolithic integrated circuit for vision and sound IF signal processing in TV and VTR sets.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 20)	4.5	5	8.8	V
I_P	supply current	51	60	69	mA
$V_{i\,IF}$	vision IF input signal sensitivity (RMS value, pins 1 and 2)	–	50	90	μV
	maximum vision IF input signal (RMS value, pins 1 and 2)	70	150	–	mV
G_v	IF gain control	64	70	73	dB
$V_{o\,CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	1.7	2.0	2.3	V
B	–3 dB video bandwidth on pin 7	6	8	–	MHz
S/N (W)	signal-to-noise ratio weighted; for video	56	59	–	dB
$\alpha_{0.92/1.1}$	intermodulation attenuation	56	62	–	dB
$\alpha_{2.76/3.3}$		56	62	–	dB
α_H	suppression of harmonics in video signal	35	40	–	dB
$V_{o\,AF}$	maximum AF output signal for THD < 1.5% (RMS value, pin 9)	0.8	–	–	V
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9800	20	DIL	plastic	SOT146(1)
TDA9800T	20	mini-pack	plastic	SOT163A(2)

Note

1. SOT146-1; 1996 December 6.
2. SOT163-1; 1996 December 6.

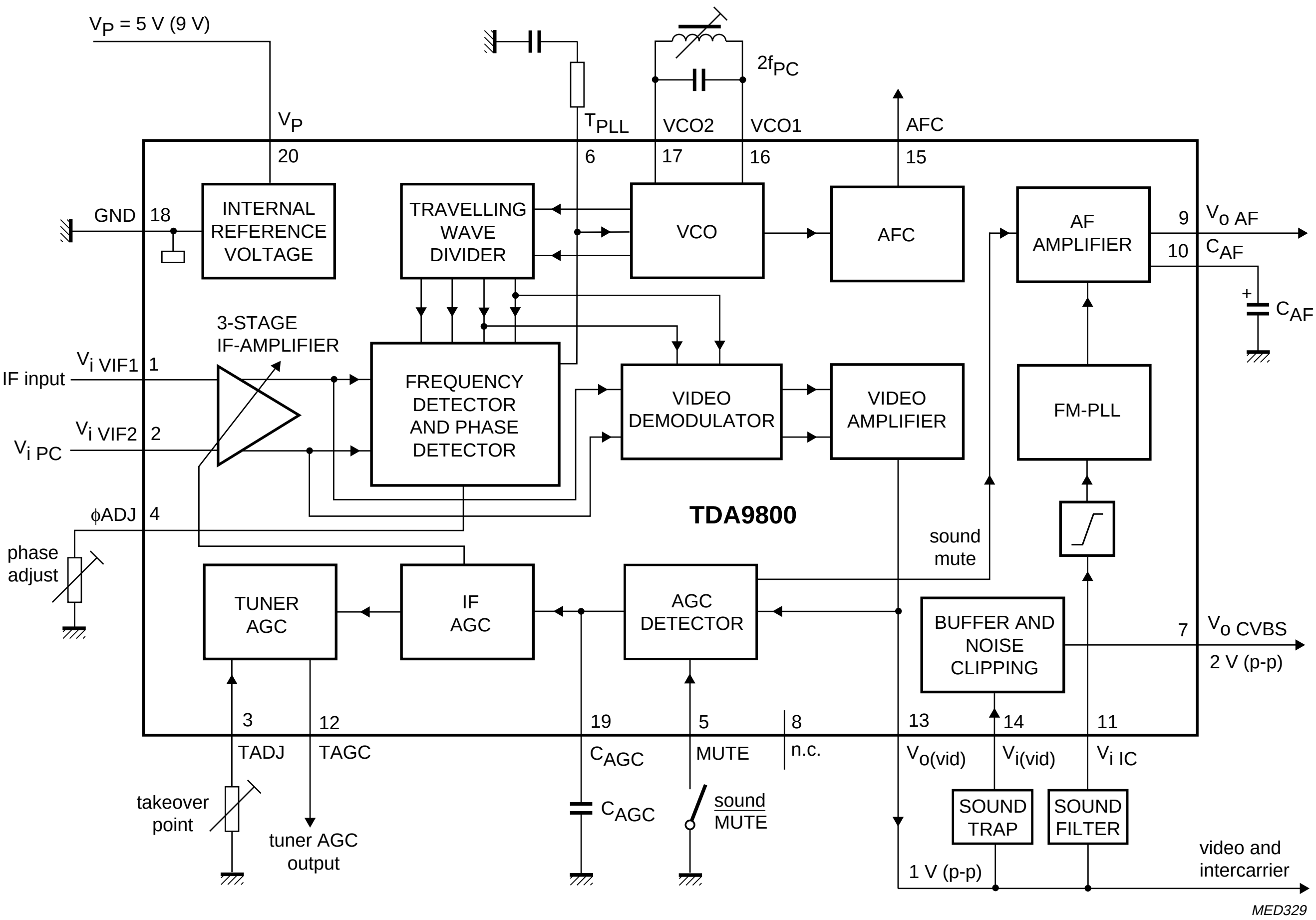


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ IF}$	1	vision IF differential input signal
	2	
TADJ	3	tuner AGC take-over adjust (TOP)
ϕADJ	4	phase detector adjust
MUTE	5	sound mute switch
T_{PLL}	6	PLL time constant of phase detector
$V_{o\ CVBS}$	7	CVBS (positive) output signal
n.c.	8	not connected
$V_{o\ AF}$	9	audio frequency output signal
C_{AF}	10	decoupling capacitor of audio frequency amplifier
$V_{i\ IC}$	11	sound intercarrier input signal
TAGC	12	tuner AGC output
$V_{o\ VID}$	13	video and sound intercarrier output signal
$V_{i\ VID}$	14	video input signal to buffer amplifier
AFC	15	automatic frequency control output
VCO1	16	VCO reference circuit for 2 f_{PC}
VCO2	17	
GND	18	ground (0 V)
C_{AGC}	19	AGC capacitor
V_P	20	positive supply voltage

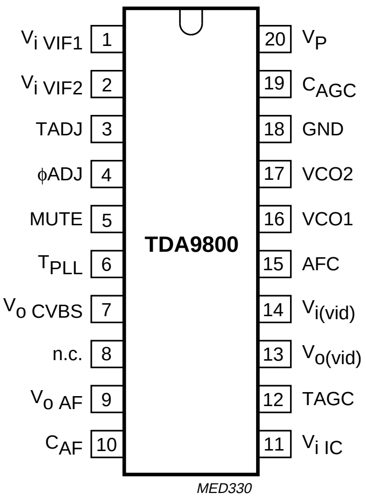


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF input

The vision IF amplifier consists of three AC-coupled differential amplifier stages; each stage comprises a controlled feedback network by means of emitter degeneration.

IF and tuner AGC

The automatic control voltage to maintain the video output signal at a constant level is generated according to the transmission standard. Since the TDA9800 is suitable for negative modulation only the peak-sync level is detected. The AGC detector charges and discharges the capacitor on pin 19 to set the IF gain and the tuner gain. The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current on pin 12 (open-collector output). The tuner AGC voltage take over point is adjusted on pin 3. This allows the tuner and the IF SAW filter to be matched to achieve the optimum IF input level.

Frequency detector, phase detector and video demodulator

The IF amplifier output signal is fed to a frequency detector and to a phase detector. During acquisition the frequency detector produces a DC current which is proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. Via the loop filter the DC current of either frequency detector or phase detector is converted into a DC voltage, which controls the VCO frequency.
The video demodulator is a linear multiplier, designed for low distortion and wide bandwidth. The vision IF input signal is multiplied by the in-phase component of the VCO output. The demodulated output signal is fed via an integrated low-pass filter (f_g = 12 MHz) to the video amplifier for suppression of the carrier harmonics.

VCO and travelling wave divider

The VCO operates with a symmetrically-connected reference LC-circuit, operating at double vision carrier frequency. Frequency control is performed by an internal varicap diode. The voltage to set the VCO frequency to the actual frequency of double vision carrier frequency, is also amplified and converted for the AFC output current.
The VCO signal is divided-by-two in a travelling wave divider, which generates two differential output signals with 90 degree phase difference independent of frequency.

Video amplifier, buffer and noise clipping

The video amplifier is a wide bandwidth operational amplifier with internal feedback. A nominal positive modulated video signal of 1 V (p-p) is present on the composite video output (pin 13). The input impedance of the 7 dB wideband buffer amplifier (with internal feedback) is suitable for ceramic sound trap filters. The CVBS output (pin 7) provides a positive video signal of 2 V (p-p). Noise clipping is provided internally.

Sound demodulation

The FM sound intercarrier signal is fed to pin 11 and through a limiter amplifier before it is demodulated. This achieves high sensitivity and high AM suppression. The limiter amplifier consists of seven internal AC-coupled stages, minimizing the DC offset.
The FM-PLL demodulator consists of an RC-oscillator, loop filter and phase detector. The oscillator frequency is locked on the FM intercarrier signal from the limiter amplifier. As a result of this locking, the RC-oscillator is frequency-modulated.
The modulating signal voltage (AF signal) is used to control the oscillator frequency. By this, the FM-PLL operates as an FM demodulator.
The audio frequency amplifier with internal feedback is designed for high gain and high common mode rejection. The low-level AF signal output from the FM-PLL demodulator is amplified and buffered in a low-ohmic audio signal output stage (pin 9). An external decoupling capacitor on pin 10 removes the DC voltage from the audio amplifier input.
By using the sound mute switch (pin 5) the AF amplifier is set to mute state.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 20) for a maximum chip temperature (note 1)			
	SOT146 at +120 °C	0	8.8	V
	SOT163A at +100 °C	0	5.5	V
V_I	voltage on pins 1, 2, 7, 11, 13, 14, 15 and 19	0	V_P	V
$t_{s\ max}$	short-circuit time	–	10	s
V_{12}	tuner AGC output voltage	–	13.2	V
T_{stg}	storage temperature range	–25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 2)	–	±300	V

Notes

1. Supply current I_P = 69 mA at T_{amb} = +70 °C.
2. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (negative and positive voltage).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	73 K/W
	SOT163A	85 K/W

CHARACTERISTICS

The following characteristics apply for V_P = 5 V; T_{amb} = +25 °C; see Table 1 for input frequencies and picture to sound ratios; V_{iIF} = 10 mV RMS value (sync level); video modulation DSB; residual carrier: 10%; video signal in accordance with CCIR line 17 or NTC-7 Composite; measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 20)	note 1	4.5	5	8.8	V
I_P	supply current		51	60	69	mA
Vision IF input (pins 1 and 2)						
V_i	input sensitivity (RMS value) at 38.9 MHz and 45.75 MHz	–1 dB video at output	–	50	90	μV
	input sensitivity (RMS value) at 58.75 MHz		–	60	100	μV
	maximum input signal (RMS value) at 38.9 MHz and 45.75 MHz	+1 dB video at output	70	150	–	mV
	maximum input signal (RMS value) at 58.75 MHz		80	160	–	mV
$\Delta V_{o\ int.}$	internal IF amplitude difference between picture and sound carrier	within AGC range; B/G: Δf = 5.5 MHz; M/N: Δf = 4.5 MHz	–	0.7	1	dB
G_{IF}	IF gain control	see Fig.4				
		38.9 MHz and 45.75 MHz	64	70	–	dB
		58.75 MHz	62	68	–	dB
B	–3 dB IF bandwidth	upper cut-off frequency	70	100	–	MHz
R_i	input resistance (differential)		1.7	2.2	2.7	kΩ
C_i	input capacitance (differential)		1.2	1.7	2.5	pF
$V_{1,\ 2}$	DC input voltage		3.0	3.4	3.8	V
True synchronous video demodulator		note 2				
f_{VCO}	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$	125	130	–	MHz
Δf_{VCO}	oscillator drift (free running) as a function of temperature	I_{AFC} = 0; note 3	–	–	±20	ppm/K
$V_{o\ ref}$	oscillator swing at pins 16 and 17 (RMS value)	f_{PC} = 38.9 MHz	–	120	–	mV
		f_{PC} = 45.75 MHz	–	100	–	mV
		f_{PC} = 58.75 MHz	–	80	–	mV
Δf_{PC}	vision carrier capture range (negative)		1.5	2	–	MHz
	vision carrier capture range (positive)		1.5	2	–	MHz
t_{acqu}	acquisition time	BL = 60 kHz; note 4	–	–	30	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i\ IF}$	IF input signal sensitivity (RMS value, pins 1 and 2)					
	for PLL still locked	maximum IF gain; note 5	–	50	90	μV
	for C/N = 10 dB	note 6	–	100	140	μV
I_{loop}	FPLL loop offset current at pin 6	note 7	–	–	±4.5	μA
Composite video amplifier (pin 13)		sound carrier off				
$V_{0\ vid}$	output signal (peak-to-peak value)	see Fig.7	0.9	1.0	1.1	V
V_{13}	sync level		1.4	1.5	1.6	V
	zero carrier level		–	2.6	–	V
	upper video clipping level		V_P – 1.1	V_P – 1.0	–	V
	lower video clipping level		–	0.3	0.4	V
$V_{0\ FM}$	IF intercarrier level (RMS value)	sound carrier on; note 8	–	170	–	mV
R_{13}	output resistance		–	–	10	Ω
I_{int13}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_{13}	maximum output sink current	DC and AC	1.4	–	–	mA
	maximum output source current		2.0	–	–	mA
B	–3 dB video bandwidth	C_{13} < 50 pF; R_L >1 kΩ	7	10	–	MHz
α_H	suppression of video signal harmonics	C_{13} < 50 pF; R_L >1 kΩ; note 9	35	40	–	dB
RR	ripple rejection on pin 13	see Fig.9	32	35	–	dB
CVBS buffer amplifier and noise clipper (pins 7 and 14)						
R_{14}	input resistance		2.6	3.3	4.0	kΩ
C_{14}	input capacitance		1.4	2	3.0	pF
V_{14}	DC voltage at input	pin 14 not connected	1.5	1.8	2.1	V
G_v	voltage gain	note 10	6	7	7.5	dB
$V_{o\ CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)	sound carrier off; see Fig.3	1.7	2.0	2.3	V
	CVBS output level	upper video clipping	3.9	4.0	–	V
		lower video clipping	–	1.0	1.1	V
		sync level	–	1.35	–	V
R_7	output resistance		–	–	10	Ω
I_{int7}	internal bias current for emitter follower	DC	1.8	2.5	–	mA
I_7	maximum output sink current	DC and AC	1.4	–	–	mA
	maximum output source current		2.4	–	–	mA
B	–3 dB video bandwidth	C_7 < 20 pF; R_L > 1 kΩ	8	11	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Measurements from IF input to CVBS output (pin 7) 330 Ω between pins 13 and 14, sound carrier off						
$V_{o\ CVBS}$	CVBS output signal on pin 7 (peak-to-peak value)		1.7	2.0	2.3	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
	black level tilt	note 11	–	–	1	%
ΔG	differential gain	CCIR line 330 or NTC-7 Composite	–	2	5	%
$\Delta\varphi$	differential phase		–	1	3	deg
B	–3 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ	6	8	–	MHz
S/N(W)	signal-to-noise ratio; weighted	see Fig.5 and note 12	56	59	–	dB
$\alpha_{0.92/1.1}$	intermodulation at ‘blue’	f = 0.92 or 1.1 MHz; see Fig.6 and note 13	56	62	–	dB
	intermodulation at ‘yellow’		58	64	–	dB
$\alpha_{2.76/3.3}$	intermodulation at ‘blue’	f = 2.76 or 3.3 MHz; see Fig.6 and note 13	56	62	–	dB
	intermodulation at ‘yellow’		57	63	–	dB
α_C	residual vision carrier (RMS value)	fundamental wave	–	1	10	mV
		harmonics	–	1	10	mV
α_H	suppression of video signal harmonics	note 9	35	40	–	dB
RR	ripple rejection on pin 7	see Fig.9	25	28	–	dB
AGC detector (pin 19)						
t_{resp}	response to an increasing amplitude step of 50 dB in input signal		–	1	10	ms
	response to a decreasing amplitude step of 50 dB in input signal		–	50	100	ms
I_{19}	charging current	note 11	0.85	1.1	1.35	mA
	discharging current		17	22	27	µA
V_{19}	AGC voltage	maximum gain	0	see Fig.4	–	V
		minimum gain	–	see Fig.4	V_P – 0.7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuner AGC (pin 12)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 22 kΩ	–	–	5	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1 and 2; R_{TOP} = 0 Ω	50	–	–	mV
V_{12}	allowable voltage	from external source	–	–	13.2	V
	saturation voltage	I_{12} = 1.7 mA	–	–	0.2	V
ΔV_{12}	variation of take over point by temperature	I_{12} = 0.4 mA	–	0.02	0.06	dB/K
I_{12}	sink current	see Fig.4				
		no tuner gain reduction	–	0.1	0.3	μA
		maximum tuner gain reduction	1.7	2.0	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 15)		see Fig.8 and note 14				
S	control steepness $\Delta I_{15}/\Delta f$	note 15				
		38.9 MHz	–0.6	–0.72	–0.84	μA/kHz
		45.75 MHz	–0.45	–0.6	–0.75	μA/kHz
		58.75 MHz	–0.38	–0.5	–0.62	μA/kHz
Δf_{IF}	frequency variation by temperature	I_{AFC} = 0; note 3	–	–	±20	ppm/K
V_{15}	output voltage upper limit	see Fig.8	V_P – 0.5	V_P – 0.3	–	V
	output voltage lower limit		–	0.3	0.5	V
I_{15}	output current source		160	200	240	μA
	output current sink		160	200	240	μA
ΔI_{15}	residual video modulation current (peak-to-peak value)		–	20	30	μA
Sound mute switch (pin 5)		note 16				
V_{IL}	input voltage for MUTE-ON		0	–	0.8	V
V_{IH}	input voltage for MUTE-OFF		1.5	–	V_P	V
I_{IL}	LOW level input current	V_5 = 0 V	–	–300	–360	μA
α_{mute}	audio attenuation	V_5 = 0 V	70	80	–	dB
ΔV_5	DC offset voltage at switching (plop)	switching to MUTE-ON	–	100	500	mV

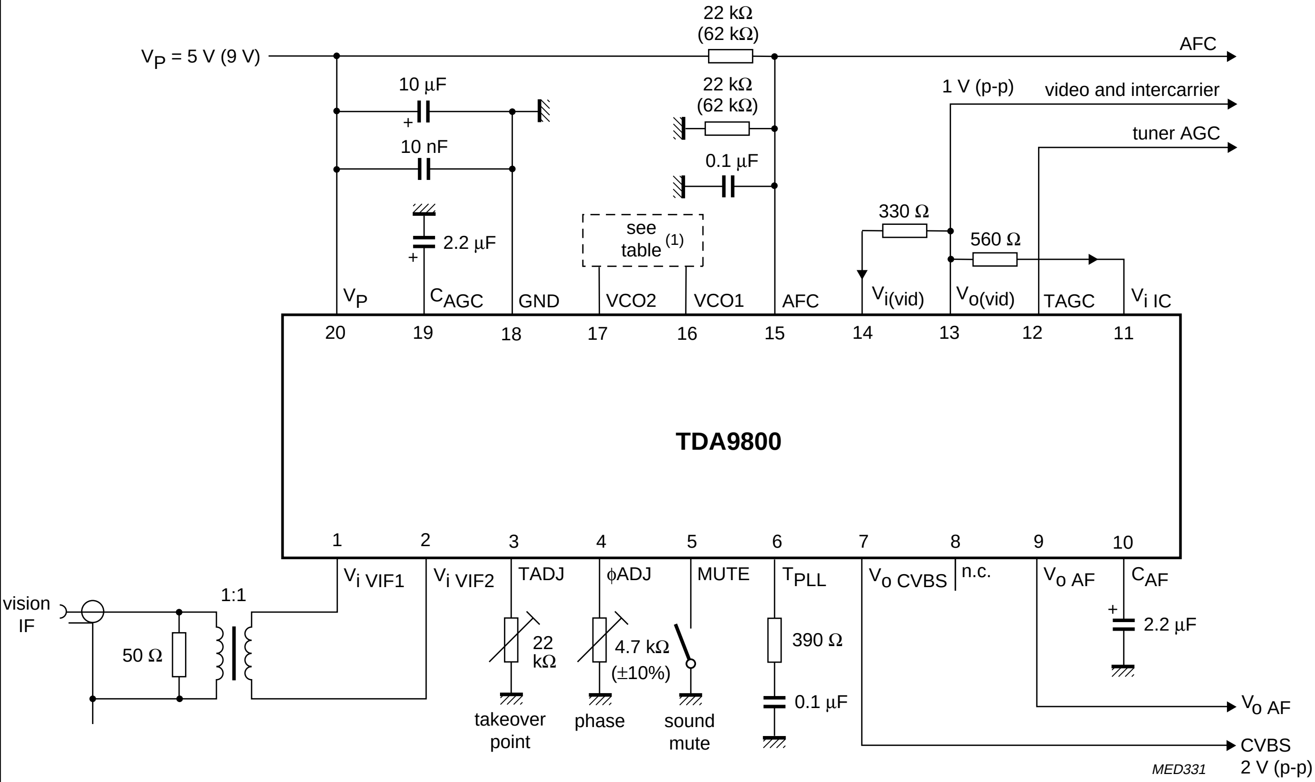
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM sound limiter amplifier (pin 11)		note 17				
$V_{i\ FM}$	input signal (RMS value, pin 11)	CCIR468-4				
	for S/N = 40 dB	see Fig.11	–	200	300	μV
	for AM suppression α_{AM} = 40 dB	AM: f = 1 kHz; m = 0.3	–	1	–	mV
	maximum input signal handling (RMS value)		200	–	–	mV
α_{AM}	AM suppression	see Fig.10; AM: f = 1 kHz; m = 0.3	46	50	–	dB
R_{11}	input resistance		480	600	720	Ω
B	–3 dB IF frequency response of sound IF	lower and upper cut-off frequency	3.5	–	10	MHz
V_{11}	DC voltage		2.3	2.6	2.9	V
FM-PLL sound demodulator and AF output (pin 9) note 17						
$f_{i\ FM}$	catching range of PLL		4	–	7	MHz
	holding range of PLL		3.5	–	8	MHz
t_{acqu}	acquisition time		–	–	4	μs
$V_{o\ AF}$	AF output signal (RMS value, pin 9)	Δf_{AF} = ±27 kHz; see Fig.11	280	350	420	mV
	maximum output signal handling	THD < 1.5%	0.8	–	–	V
ΔV_o	temperature drift of AF output signal		–	3	7	10^{-3} dB/K
Δf_{AF}	frequency deviation	THD < 1.5%; note 18	–	–	±50	kHz
V_{10}	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 19	1.2	–	2.2	V
R_9	output resistance		–	100	–	Ω
R_L	load resistance (pin 9)		2.2	–	–	kΩ
V_9	DC voltage		1.6	2.0	2.4	V
B	–3 dB audio frequency bandwidth		95	120	–	kHz
THD	total harmonic distortion	without ceramic filter	–	0.1	0.5	%
S/N (W)	signal-to-noise ratio, weighted	CCIR468-4; see Fig.11	50	55	–	dB
V_{SC}	residual sound carrier and harmonics (RMS value)		–	–	75	mV
RR	ripple rejection on pin 9	see Fig.9	26	30	–	dB
Measurements from IF input to audio output (pin 9) 560 Ω between pins 13 and 11; note 20						
S/N (W)	weighted signal-to-noise ratio	27 kHz FM deviation; CCIR468-4; 50 μs (75 μs at standard M) de-emphasis; with offset alignment on pin 4				
	6 kHz sinusoidal waveform	black-to-white	39	46	–	dB
	black picture	sync only	40	48	–	dB
	white picture		39	46	–	dB
	colour bar		39	46	–	dB

Notes

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2 calculated with grey level and FPLL input signal level). Resonance circuit of VCO: $Q_o > 50$; C_{ext} = 8.2 pF; $C_{int} \approx$ 8.5 pF (loop voltage about 2.7 V).
3. Temperature coefficient of external LC-circuit is equal to zero.
4. $V_{i\,IF}$ = 10 mV (RMS value); Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
5. $V_{i\,IF}$ signal for nominal video signal.
6. Transformer at IF input (Fig.3). The C/N ratio at IF input for ‘lock-in’ is defined as the vision IF input signal (sync level, RMS value) in relation to a superimposed, 5 MHz band-limited white noise signal (RMS value); video modulation: white picture.
7. Offset current measured between pin 6 and half of supply voltage (V = 2.5 V) under the following conditions: no input signal at IF input (pins 1 and 2) and IF amplifier gain at minimum ($V_{19} = V_P$), pin 4 (phase adjust) open-circuit.
8. The intercarrier output signal is superimposed to the video signal at pin 13 and can be calculated by the following formula: $20\log\left(\frac{V_{13\ interc.}\ (p\text{-}p)}{1V\ (p\text{-}p)}\right) = \frac{V_{iSC}}{V_{iPC}}\ dB + 6.9\ dB \pm 2\ dB$ with $\frac{V_{iSC}}{V_{iPC}}\ dB$ = sound to picture carrier ratio at IF input (pins 1 and 2 in dB and ±2 dB = tolerance of intercarrier output amplitude $V_{o\,FM}$.
9. Measurements taken with SAW filter G1962; modulation: VSB, $f_{video} > 0.5$ MHz, loop bandwidth BL = 60 kHz.
10. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 13 to pin 14).
11. The leakage current of the AGC capacitor has to be < 1 μA to avoid larger tilt.
12. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 7). B = 5 MHz weighted in accordance with CCIR-567 at a source impedance of 50 Ω.
13. $\alpha_{0.92/1.1}$ = 20 log (V_o at 4.4 (3.58) MHz / V_o at 0.92 (1.1) MHz) + 3.6 dB; $\alpha_{0.92/1.1}$ value at 0.92 (1.1) MHz related to black/white signal.
    $\alpha_{2.76/3.3}$ = 20 log (V_o at 4.4 (3.58) MHz / V_o at 2.76 (3.3) MHz); $\alpha_{2.76/3.3}$ value at 2.76 (3.3) MHz related to colour carrier.
14. To match the AFC output signal to different tuning systems a current source output is provided (Fig.8).
15. Depending on the ratio $\Delta C/C_o$ of the LC resonance circuit of VCO ($Q_o > 50$; $C_o = C_{int} + C_{ext;}$ C_{ext} = 8.2 pF; $C_{int} \approx$ 8.5 pF).
16. No mute state is also valid for pin not connected.
17. Input level for second IF from an external generator with 50 Ω source impedance, AC coupled with 10 nF capacitor, f_{mod} = 1 kHz, 27 kHz (54% FM deviation) of audio reference. A VIF/SIF input signal is not permitted. Pin 19 has to be connected to positive supply voltage. S/N and THD measurements are taken at 50 μs (75 μs at standard M) de-emphasis.
18. To allow higher frequency deviation, the resistor R_x on pin 10 (see Fig.12) has to be increased to a value which does not exceed the AF output signal of nominally 0.35 V for THD = 0.1% (R_x = 4.7 kΩ provides –6 dB amplification).
19. The leakage current of the 2.2 μF capacitor is < 100 nA.
20. For all S/N measurements the used vision IF modulator has to meet the following specification:
    - Incidental phase modulation for black-to-white jump less than 0.5 degree.

Table 1 Input frequencies and carrier ratios.

		B/G STANDARD	M/N STANDARD	M STANDARD	UNIT
picture carrier	f_{PC}	38.9	45.75	58.75	MHz
sound carrier	f_{SC}	33.4	41.25	54.25	MHz
picture to sound carrier ratio	SC	13	7	7	dB



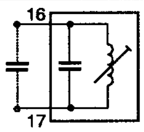
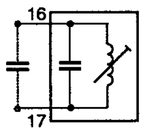
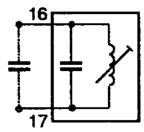
PARAMETER	EUROPE	USA	JAPAN
IF frequency	38.9 MHz	45.75 MHz	58.75 MHz
VCO frequency	77.8 MHz	91.5 MHz	117.5 MHz
oscillator circuit	 C(VCO) C L 8.5 pF 8.2 pF 251 nH	 C(VCO) C L 8.5 pF 10 pF 163 nH	 C(VCO) C L 8.5 pF 12 pF 90 nH
e.g. TOKO coil Philips ceramic capacitor	5KM 369SNS-2010Z 222263251828	5KMC V369SCS-2370Z (inside of coil)	MC139 NE545SNAS100108 12 pF SMD size = 0805

Fig.3 Test circuit.

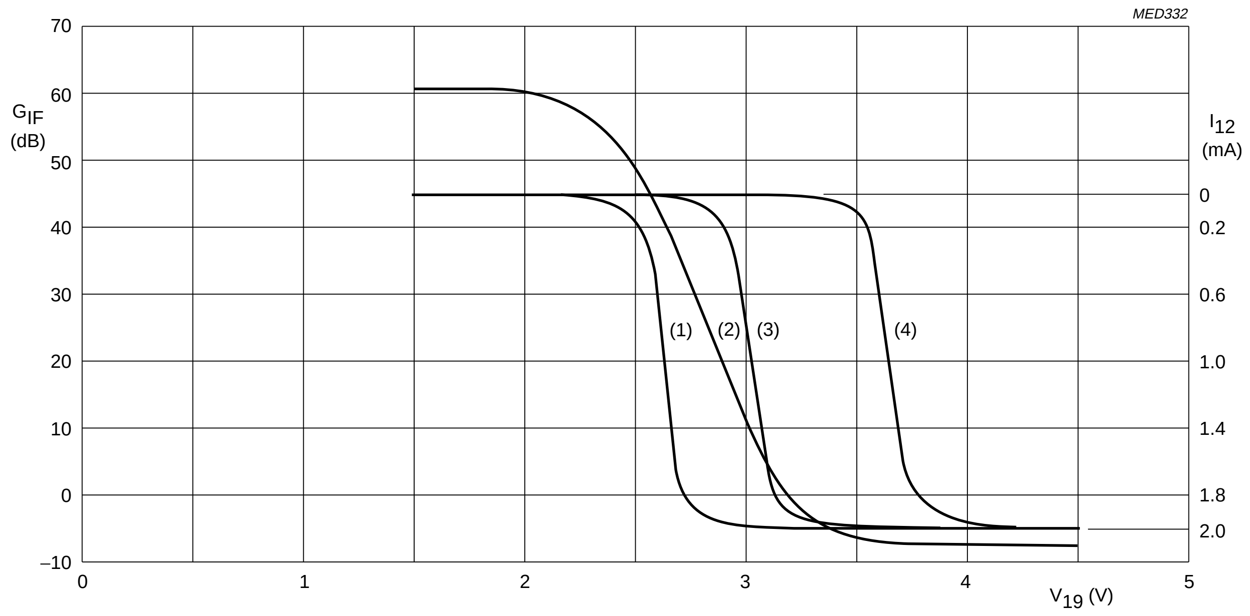


Fig.4 IF AGC (dashed) and tuner AGC as a function of take over point adjustment.

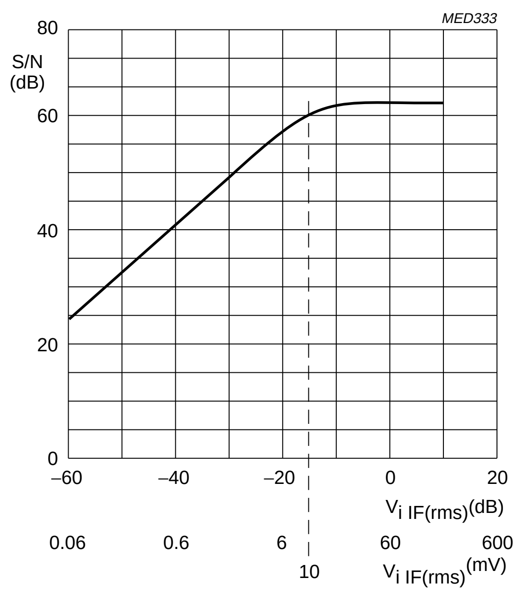
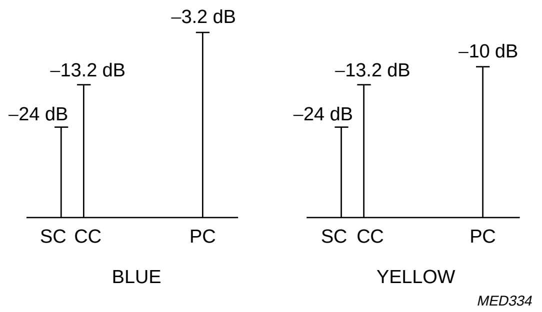


Fig.5 Typical signal-to-noise ratio as a function of IF input signal.



SC = sound carrier level ; with respect to TOP sync level.
CC = chrominance carrier level ; with respect to TOP sync level.
PC = picture carrier level ; with respect to TOP sync level.

Sound shelf attenuation: 17 dB.

Fig.6 Input conditions for intermodulation measurements.

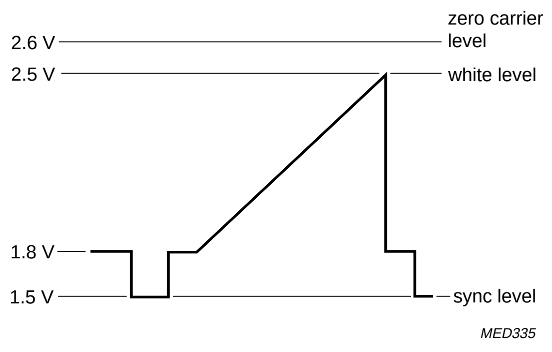


Fig.7 Video signal levels on output pin 13.

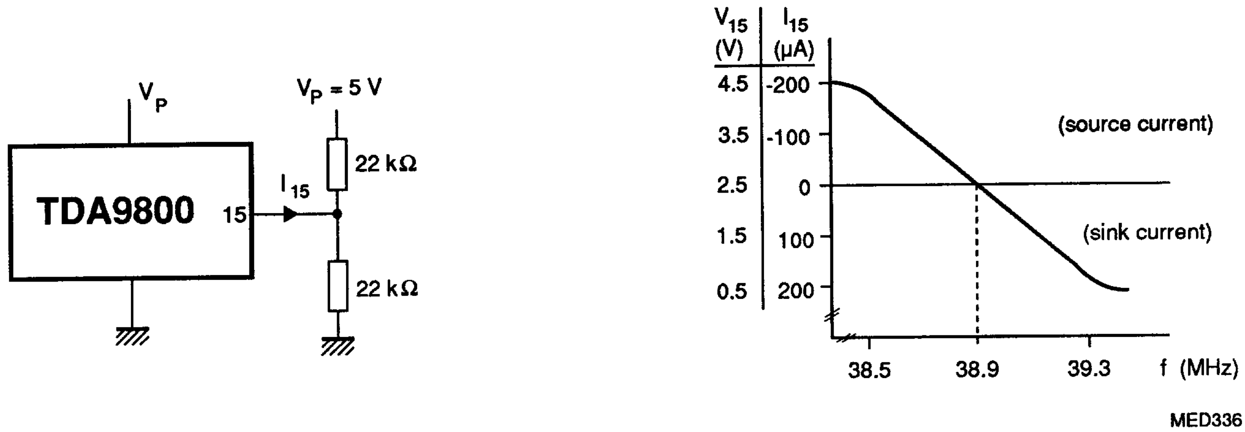


Fig.8 Measurement conditions and typical AFC characteristic.

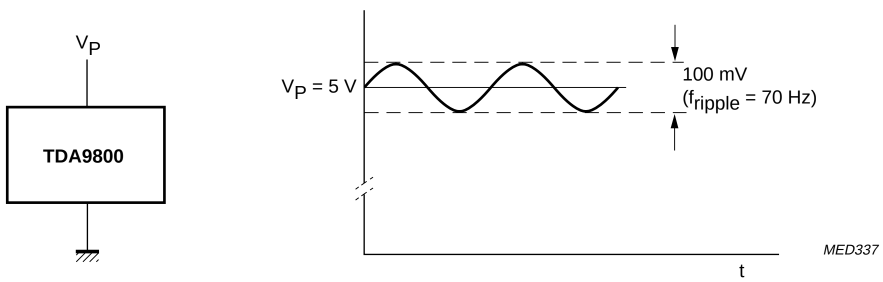


Fig.9 Ripple rejection condition.

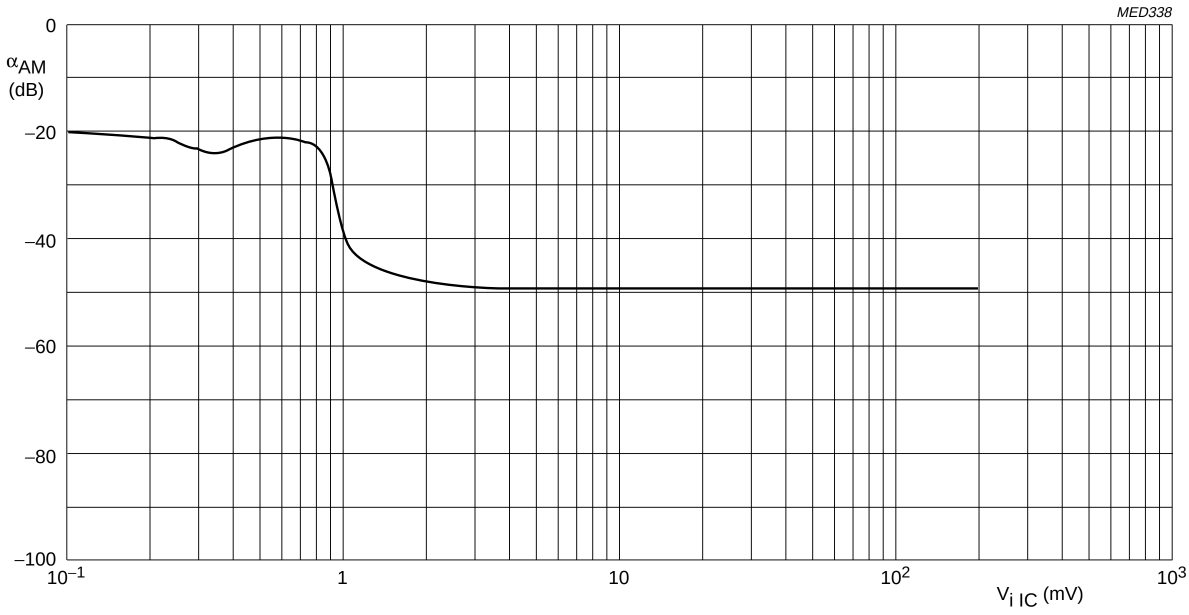


Fig.10 Typical AM suppression of FM sound demodulator.

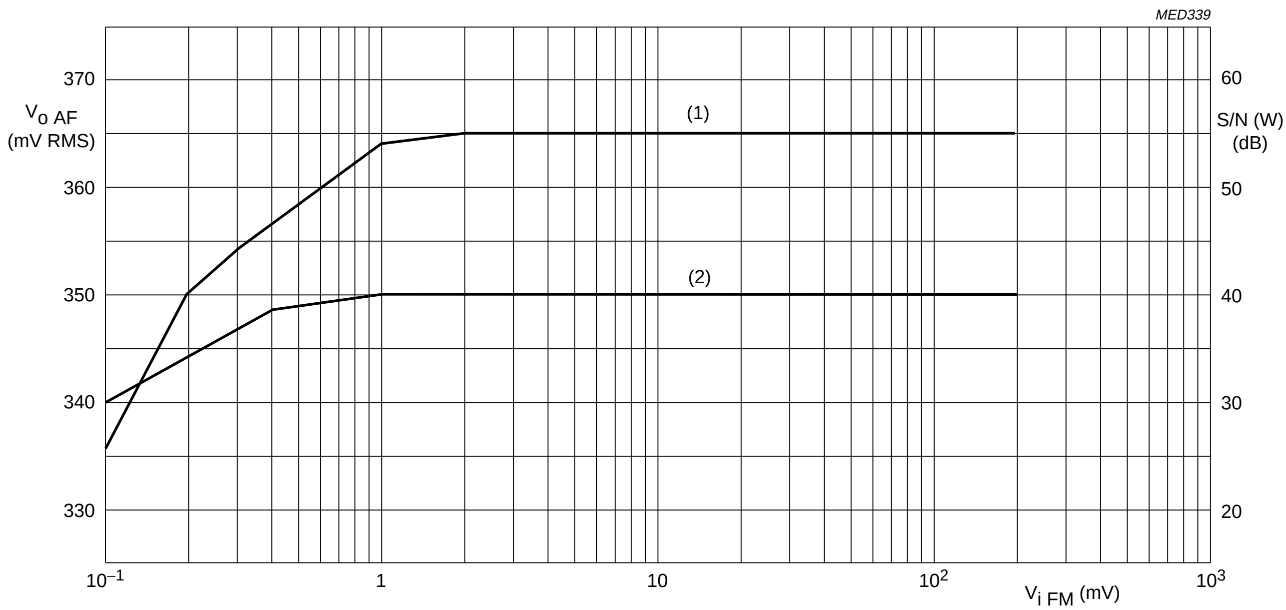
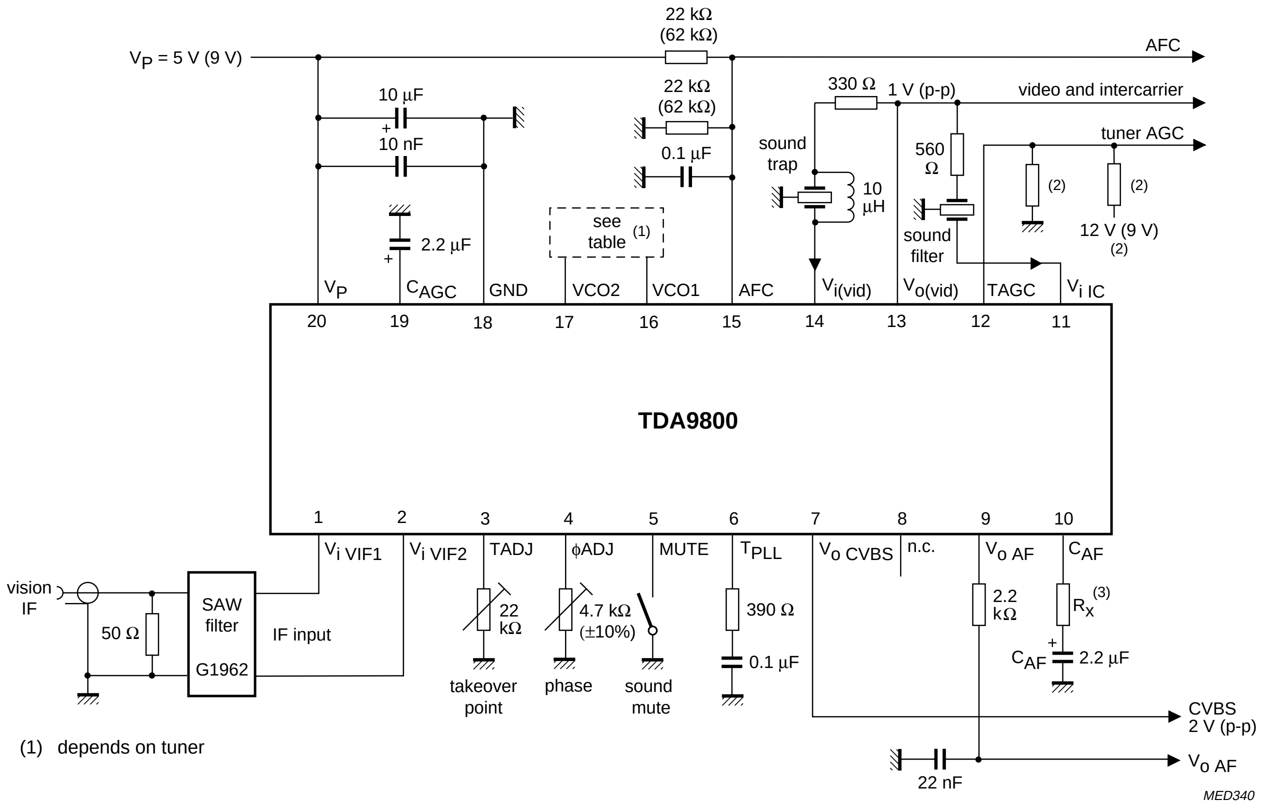


Fig.11 Typical AF output signal and signal-to-noise ratio.



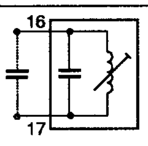
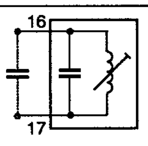
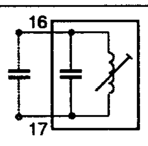
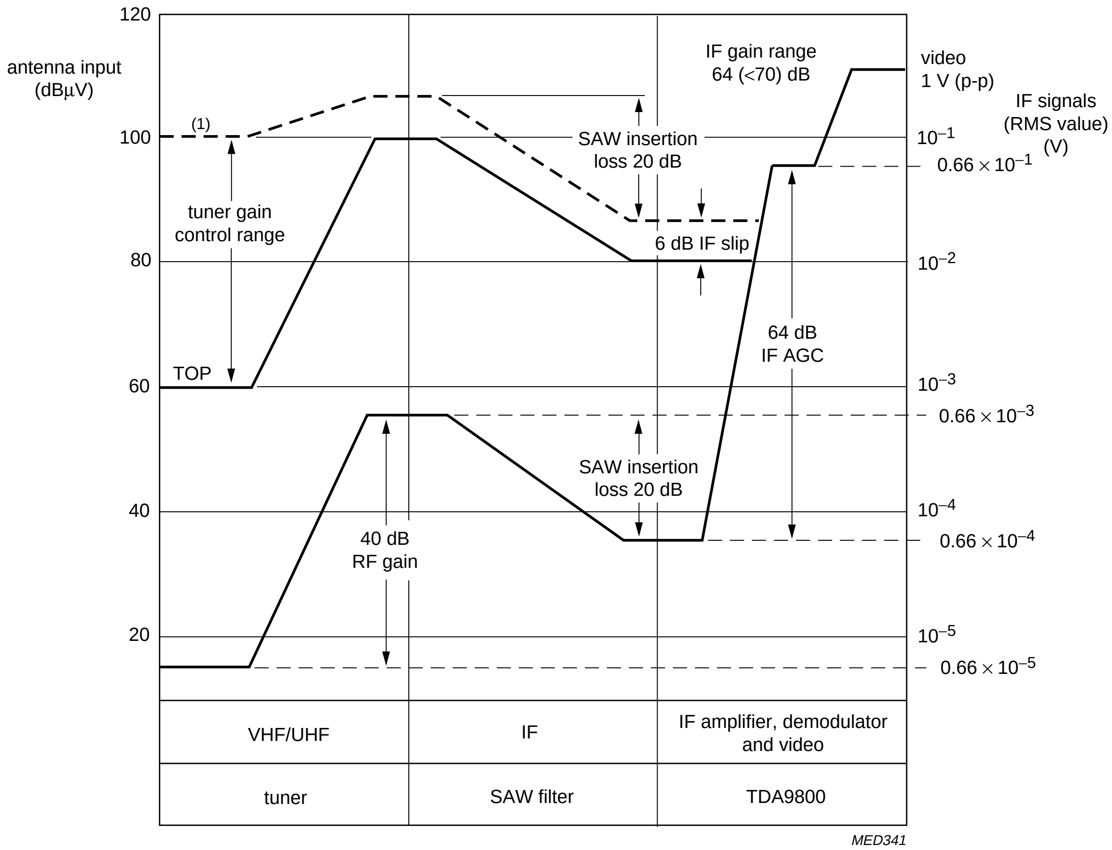
PARAMETER	EUROPE	USA	JAPAN
IF frequency	38.9 MHz	45.75 MHz	58.75 MHz
VCO frequency	77.8 MHz	91.5 MHz	117.5 MHz
oscillator circuit	 C(VCO) C L 8.5 pF 8.2 pF 251 nH	 C(VCO) C L 8.5 pF 10 pF 163 nH	 C(VCO) C L 8.5 pF 12 pF 90 nH
e.g. TOKO coil Philips ceramic capacitor	5KM 369SNS-2010Z 222263251828	5KMC V369SCS-2370Z (inside of coil)	MC139 NE545SNAS100108 12 pF SMD size = 0805

Fig.12 Application circuit.



(1) depends on TOP

Fig.13 Front end level diagram.

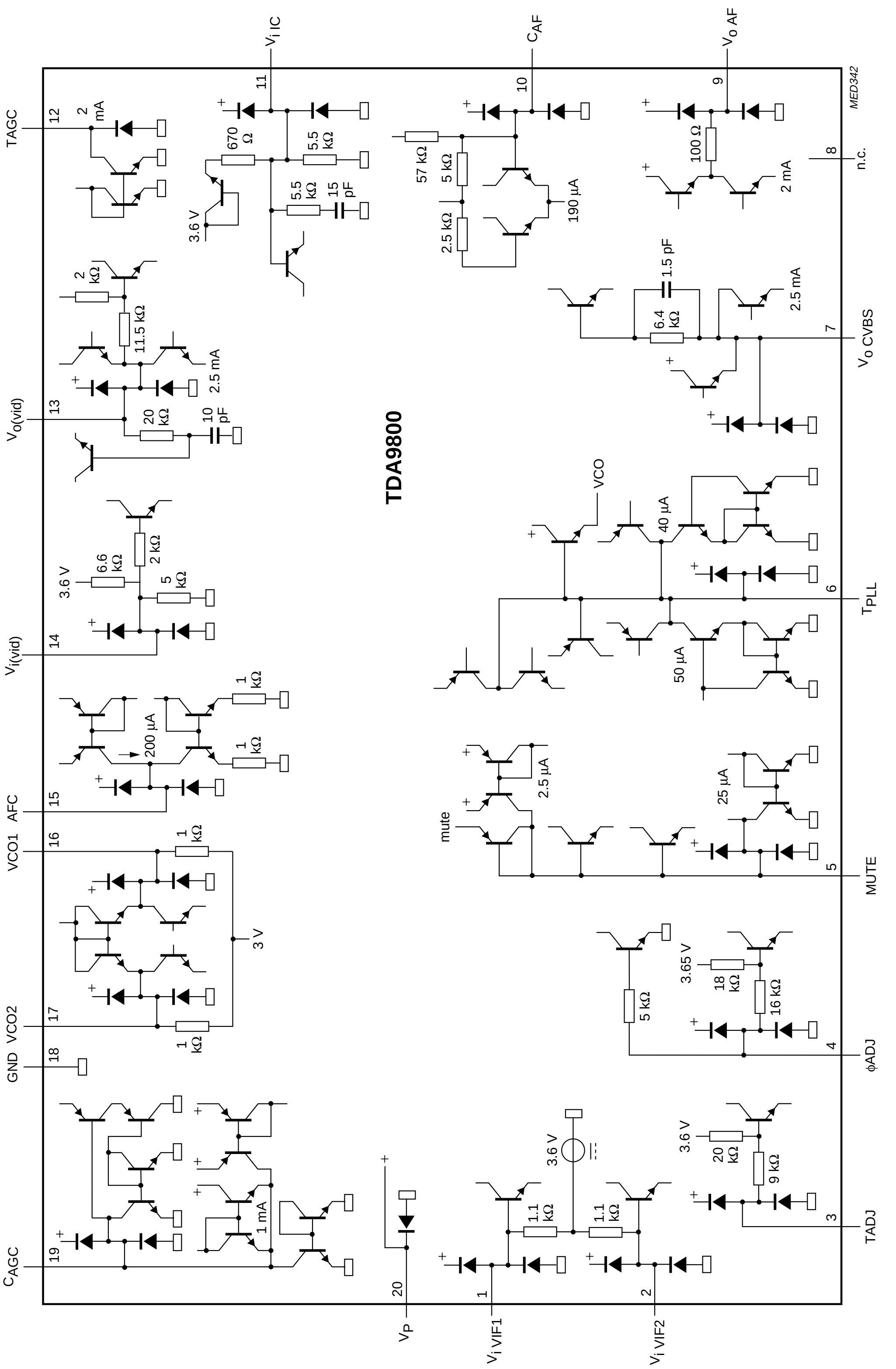
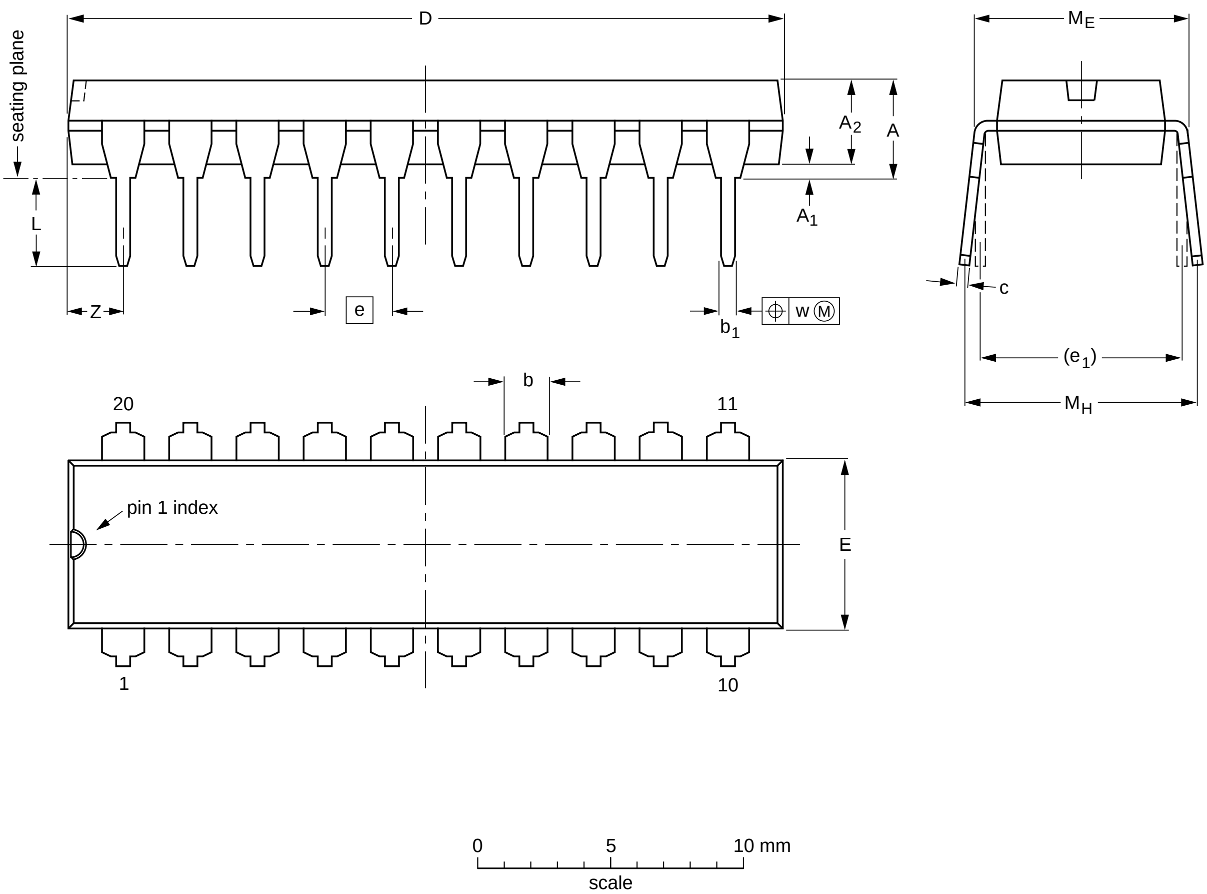


Fig.14 Internal circuits.

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

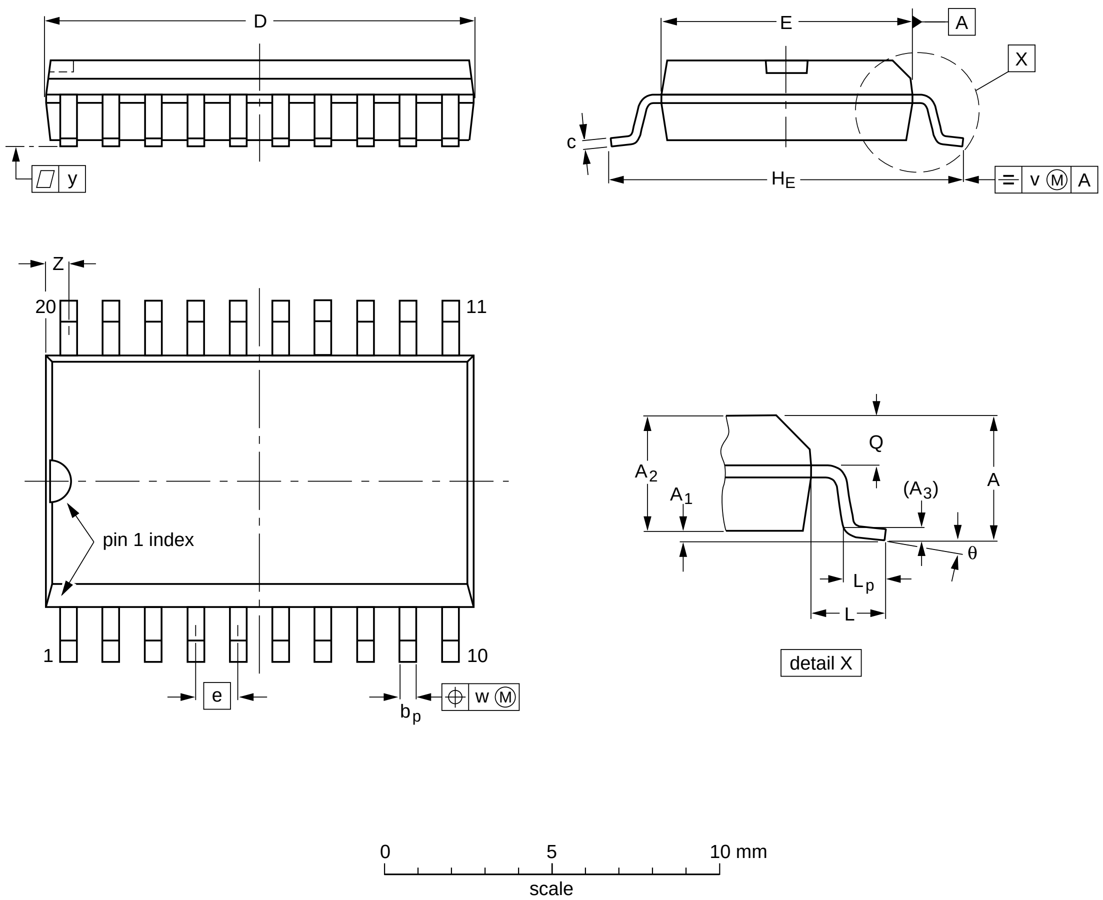
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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